ABSTRACT OF THE DISCLOSURE

A display driver circuit includes first to Mth SR blocks which are disposed in a region on the right side of a data input control circuit and hold first to Mth gray-scale data, and (M+1)th to (M+N)th SR blocks which are disposed in a region on the left side of the data input control circuit and hold (M+1)th to (M+N)th gray-scale data. The first to (M+N)th SR blocks hold the first to (M+N)th gray-scale data for which mask control is performed based on a data enable signal shifted by each SR block. The first to Mth gray-scale data is masked in order from first to Mth data mask circuit. The (M+1)th to (M+N)th gray-scale data are unmasked in order from (M+1)th to (M+N)th data mask circuit.